REMARKS

Claims 1-30 were pending in the present application. Claims 8, 18, and 28 have been cancelled. Claims 1, 9, 11, 19, 21, and 29 have been amended. Accordingly, claims 1-7, 9-17, 19-27, 29, and 30 remain pending in the application.

Claims 1-30 stand rejected under 35 U.S.C. §102(b) as being anticipated by Liencres et al. (U.S. Patent No. 5,434,993) (hereinafter " Liencres"). Although Applicant respectfully traverses at least portions of this rejection, Applicant has amended the claims to expedite alowance.

Applicant's claim 1 as amended recites a node comprising in pertinent part,

> "an address network configured to convey address packets between the interface and the plurality of active devices; and
>
> a data network configured to convey data packets between the interface and the plurality of active devices, wherein the address network and the data network are **separate** networks each including a respective plurality of communication links;
>
> ...
>
> ...wherein the interface is configured to send a proxy address packet on the address network in response to receiving the request from the another node, wherein the active device is configured to store a promise corresponding to the proxy address packet in a promise array included in the active device in response to receiving the proxy address packet **while having the ownership responsibility** for the coherency unit, **but not having the data** corresponding to the coherency unit; and
>
> wherein the promise comprises information that identifies a particular data packet that needs to be forwarded, and the destination to which the data packet must be forwarded." (Emphasis added)

Applicant submits, Liencres does not teach or disclose anywhere, a separate address and data network as recited in Applicant's claim 1.

In the rejection of claim 8, the Examiner asserts Liecres teaches the promise being stored within a promise array within the active device at as element 46 (no other description is provided). Applicant respectfully disagrees. More particularly, element 46 in Liencres is a bus cache controller directory within the bus controller 31. Liencres discloses at col. 9, lines 14-32

> "The processor cache directory 34 and the bus cache controller directory 46 store the address tags and status bits for the information in the cache memory 37. The address tags and status bits in the processor cache directory 34 and the bus cache controller directory 46 usually match. However, the address tag and status bits for a given cache line in the processor cache directory 34 and the bus cache controller directory 46 may not correlate at all times. For example the processor cache controller 35 may have written back a subblock from a cache line to the bus cache controller 31 so the processor cache controller 35 no longer "owns" the subblock, but the bus cache controller 31 does still own the subblock. When the bus cache controller 31 issues a request for the new information and transfers control of the old subblocks to the pending write-back controller 40, the bus cache controller directory 46 again matches the processor cache directory 34." (Emphasis added)

From the foregoing, Applicant submits the bus cache controller directory 46 only stores address tags and status bits that correspond to information in the cache memory 37. This is different than an active device maintaining a storage array that stores (a promise) information that identifies data packets that need to be forwarded and the destination. In addition, the promise is stored in resposne to receiving a proxy adress packet for the data which it owns but does not currently have. Applicant submits this is not taught anywhere in Liencres.

Accordingly, Applicant submits claim 1, along with its dependent claims, patentably distinguishes over Liencres for the reasons given above.

Applicant's claims 11 and 21 recite features that are similar to the features recited in claim 1. Thus Applicant submits claims 11 and 21, along with their respective dependent claims, patentably distinguish over Liencres for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-99001/SJC.

Respectfully submitted,

/ Stephen J. Curran /
Stephen J. Curran
Reg. No. 50,664
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

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